Customer No.: 31561
Docket No.: 11555-US-PA
Application No.: 10/605,099

AMENDMENTS

In The Title

Please amend Title by substituting with

--PIPELINE ACCESSING METHOD TO A LARGE BLOCK MEMORY--

In The Specification

[0014] As embodied and broadly described herein, the invention provides [[a]]an accessing method to a large block flash memory is described. The large block flash memory has a plurality of pages and each page has a plurality of sectors[[~~-by-N~~]]. The memory device has a controller to control an access operation between a host and a large block memory of the memory device with a page buffer. The controller includes at least two buffers, when the host intends to program the memory device. In the method, data sectors are transferred between the host and the large block flash memory by alternatively using the buffers. After transferring N data sectors with respect to one page, a start program command is issued by the controller for programming the memory cell array. Wherein the data transferring operation is using a pipeline manner and is divided into three stages. At least two of the three stages can be performed at the same time. Wherein the memory device has two page buffers, which are also arranged into a pipeline to receive the pages in faster operation speed.

[0016] The invention also provides a method of accessing a large block flash memory, wherein the large block flash memory has a plurality of pages and each page has a plurality of sectors[[~~-by-N~~]]. The memory device has a controller to control an access operation between a host and a large block flash memory of the memory device. The controller also has two buffers regions. The method comprises transferring a portion of a current page data from the host to the controller, and transferring a portion of the current page data from the controller to the data cache, wherein the two transferring steps can be

performed at the same time. The current page data in the data cache is then shifted to the page buffer. And, the current page data is programmed into the memory cell array, and simultaneously the foregoing two transferring steps are performed if a next page data is desired to continuously transfer.